With the increasing use of electronics in a wide range of applications, it is imperative to keep the pace of product design high, while maintaining the quality of output. Consumer electronic gadgets continue to see an increased level of innovation as form factors become slimmer; even as multiple features are being packed in the same design. Consumers have come to expect the features seen in multiple gadgets five years ago be offered in a single device today.

To enable the level of integration demanded, the industry has moved to deep-sub-micron (DSM) processes. Older technology nodes (0.18um and above) do still find useful applications in precision analog and high voltage applications including power management, audio and display drivers. However, the nature of challenges faced in the analog and mixed signal designs have changed with process nodes, while some of the design challenges associated with the older geometries have increased with more functionality being added.

**DSM Challenges**

As technology has advanced to DSM, the number of effects on transistor characteristics has increased. While one could reasonably calculate device parameters, such as transconductance by hand in 0.25um and above technologies, it is nearly impossible in DSM. One has to do with trends and simulations only. This is due to increased non-idealities, making the relationship between drain current and gate-to-source voltage complex (from nearly a square relationship). As gate oxide thickness and channel lengths have reduced, the voltage that can be handled across these terminals has come down. The core devices, which previously could handle 1.2V in 130nm devices, can now handle 0.9V in 28nm. The drop in voltage reduces the headroom for analog circuits. Use of dual gate oxides (IO and core) have been popular for quite some time (including the use of drain extended transistors) to get better signal fidelity. But constraints in system design require some of the designs to work off of lower supplies. Architectures to work at lower supply
have been developed, but typically come at the cost of more power and area. One of the most important aspects of analog design is the desire to maintain or enhance signal fidelity. Noise generated by the circuit has to be kept at a minimum at reasonable power consumption levels. When the channel lengths were large, the thermal noise of a metal oxide semiconductor (MOS) transistor could be derived, assuming the channel to be resistive when in deep inversion. This led to a fairly simple model, which could be used in hand analysis for further optimization. As channel lengths have narrowed, high field effects have increased the noise more than that predicted by thermal (resistive) considerations alone. The gate leakage current also introduces a noise component, which has to be accounted for in noise budgets.

Device matching is another phenomenon needing close attention in DSM processes. While matching non-idealities due to manufacturing have been reduced in DSM, other electrical issues have surfaced. Gate leakage currents have increased considerably in 28nm and below, and warrant a closer look at how this affects the matching of devices. No longer can the designer just scale the gate area to improve matching. The increased area increases the leakage current, which will introduce some mismatch. Thus there will be a limit to the achievable accuracy for a given power level. Circuits that depend on current matching, such as digital to analog convertors (DACs) or current mirrors, will have to either revisit optimization constraints to accommodate increased leakage, or stick to using IO devices for current sources.

The shallow trench isolation (STI) stress effects can change the current in MOS devices by as much as 20 percent. This STI effect depends on the distance of the active channel to the STI region, as shown in Figure 1A. Thus, it is imperative that the transistor be laid out as it was simulated. If not, the transistor parameters must be extracted post layout and checked for STI effects before doing final back annotation runs (which can be time consuming).

While STI impact on the transistor is predominantly its own property, the well proximity effect (WPE) depends on the surroundings of the transistors. The impact of well doping ions scattered by the photo resist, as shown in Figure 1B, causes a gradation in the doping profile of the wells. This causes both the threshold voltage (Vt) to increase and a reduction in current. These effects cannot be incorporated into the schematic without knowledge of how the layout will be floor planned. Therefore, it is necessary to take care of this effect while doing layout for critically matched transistors, or for which the absolute drive strength is important.

With reducing lengths, the drain and source depletion region in a MOS transistor accounts for a significant portion of the channel charge, as shown in Figure 1C. This causes an increase in drain current at a given gate to source voltage. This phenomenon is often referred to as drain induced barrier lowering (DIBL). It also reduces the output resistance of the device, more than what is predicted by the channel length modulation. In turn, this reduces the gain of the transistor. Even when the transistor is off (gate to source voltage is 0), the depletion region caused by the drain source voltage increases the current flow. This increase in leakage current increases the power consumed in mixed signal designs. Multiple design and process techniques have been evolved to combat this leakage current increase.
in DSM processes, some of which include back bias, power gating, non-use of low-length devices in non-critical areas, multi Vt device and libraries, among others.

**Layout Challenges**

As critical dimensions are reduced in DSM processes, gate lengths are also reduced. This brings up another issue in transistor layouts. For narrow-length transistors, the gate resistance of the transistors has increased. This limits the maximum width of the transistors that can be used effectively in high-speed circuits. For large-width devices, it becomes necessary to create multi-finger devices, with the gate contacted at both ends of the transistor. The resultant WPE and STI effects must be given importance at the design phase itself, so as not to create surprises in critical circuits post-layout.

With decreasing metal thickness in DSM processes, the resistivity of the metal layers has gone up and the electro-migration limits have come down. Power networks, high current paths in analog circuits and high-speed paths have to be laid out with more care. Similar care has to be extended to vias and contacts.
With decreasing oxide thickness, the capacitance-per-unit area of MOS devices has increased. For normal circuits, this can be seen as a limitation, but for a class of analog circuits, this is a good thing. Ability to realize large capacitances helps in filtering applications for signals, as well as for power. Effectively used, the area for a given capacitance does come down. However an additional manufacturing issue can limit the amount of gain. The poly density in DSM processes below 40nm stands around 50-65 percent, limiting the amount of capacitance per unit area.

Further, the restriction to use gate poly in only one orientation, due to better manufacturability, has restricted the amount of gains from an area perspective. This also has forced intellectual property (IP) vendors to give their IPs in two orientations, forcing an increased layout and verification effort.

Simulation Challenges

With the increase in design complexity in DSM processes due to physical effects, as well as effects due to feature length reduction, it has become necessary to estimate the robustness of the circuit. Typically, this has been done by varying the process, voltage, temperature and external component value variations, leading to thousands of simulation runs. The variability analysis also has to be carried out, typically where performance is on the margin. Another approach is to use Monte Carlo simulations with global and local variations accounted for. Using these simulations, along with advanced methodologies, it is becoming possible to reduce the number of runs required to find worst case corners and take corrective actions.

To combat the loss of gain or matching limitations due to gate leakage, digital calibration techniques are generally used. These are also used to tune oscillators, resistors and capacitors at the component level, and channel equalization at a system level. Digital aid has helped extend the utility of analog circuits, while helping lower power. To verify the functionality of the calibration, checks are usually performed with the analog modeled in HDL. To verify the performance, mixed mode simulations are generally used with the digital in HDL and the rest of the analog circuit at transistor level. These simulations tend to be slow, as the analog is simulated in a full accuracy simulator. It is therefore essential to get the behavior of the functional models of the analog correct. This is easier said than done, as there is no methodology, unlike in the digital world, to verify the correctness automatically. It depends both on the accuracy of the person developing the circuit and on the behavior model to get it right for all of the cases. One approach is to develop functional models at smaller block levels. This ensures that the number of modes that need to be incorporated in the model are low and that the connectivity of the analog portion is also verified.

Many chips these days have switching power circuits integrated with sensitive analog. These need to be simulated with package parasitics and external components. Package parasitic is typically dominated by inductances. Simulators tend to be a lot slower when these inductances are added in the simulation netlist. It is common for simulators to take four to five days per simulation when there are two switching power converters along with an oscillator, a low-resolution data converter, IO and ESD and small associated logic, shown in Figure 2. These are despite the dramatic simulation speed gains in the last few years.
(with the aid of multi-cpu, multi-threading simulators). The gains are not enough to be able to run large simulations and use them to improve the design further in aggressive tape out schedules.

ERC Checks

Apart from the parameters that can be simulated, there are a class of checks that cannot be caught by simulations (identifying electrically floating nodes in the design). It then becomes necessary to develop scripts around the simulation netlist to test for these. These issues typically arise in designs that use multiple voltage domains to reduce power. If the designer is not careful, the design will end up taking more current than it was designed for.

For circuits that interact with the external world, it is necessary to understand the electro static discharge (ESD) and latch up (LU) requirements before the design is started. These do place several restrictions on the output and input stages of the design. However, these are well known, and guidelines are generally provided in process documents. It is also necessary to check the internal components of the circuit for ESD tolerance, and if there is a high frequency path from the output or input to some intermediate node of the circuit. Simple simulations can show the ESD tolerance and it is advisable to incorporate these early into the design cycle to avoid surprises later. Apart from these, the choice of ESD circuits and interaction with other circuits due to the ESD ring have to be accounted for. Only
simulations at the top level can help understand these, provided a good model of the ESD circuits are available.

**Conclusion**

With movement to 20nm and then onto 14nm technologies within the next five years, the complexity to mixed signal designs will increase. Specifically, analog circuits will have to deal with lower gain leaky devices, which will necessitate active digital calibration circuits. Reliability and variations will need closer attention, as these will dominate the design process and performance. Tools for critical analog layout to aid in better matching and reduce variations directly from the schematic will be needed. As the resistance of metals increase, resistive back annotation will also be essential to close the design. Algorithms to predict performance degradation at the schematic level itself will be needed. In fact, more layout non-idealities will be annotated in the schematic itself to help reduce post layout issues. Simulation times will increase with an increase in design complexity. Hardware accelerators for analog simulators or simulators optimized for GPUs to get speed advantage will be required. On the digital side, and apart from known issues, high energy particle radiation related issues will start to appear. Designs will see more upsets due to the smaller critical charge. Design techniques to deal with these will become mainstream (from the more esoteric areas of space hardened designs today). There will be plenty of opportunities to innovate and make interesting advances in mixed signal designs.

**About the Author**

C.Srinivasan received his BT in electronics and communications from IIT Chennai in 1989. He then worked with the H/W R&D Centre, HCL for 18 months until February, 1991. That same month, he joined Texas Instruments, Bangalore, in the mixed signal design group. In his 14 years of association with TI, he worked in a variety of fields, beginning with analog modeling. He then led a team to develop data converters, and was responsible for putting TI in a leadership position for SAR ADC products with resolutions up to 18bits and speeds up to 1MSPS. In 2005, he co-founded Cosmic Circuits focusing on analog and mixed-signal designs. As VP, engineering, he has set-up the team to execute a variety of analog IPs including power management chips, data converters, analog front ends, PLLs, serial interfaces and analog ASICs. He has also authored three international papers and has five patents in his name.